REMARKS/ARGUMENTS

Claims 1-5 and 9-15 were rejected over Ban in view of Higuchi et al. Claims 6-8 were rejected over Ban, Higuchi and Crawford et al. Claims 17-20 were rejected over Ban, Higuchi and Horn et al.

Allowable Subject Matter

Claim 16 was found to recite allowable subject matter in the Office Action dated September 3, 2008. This claim is being rewritten in independent form as new claim 21, reciting the features of claims 1, 15 and 16 as presented in the Preliminary Amendment dated July 19, 2006. Claim 16 is also being placed in independent form, as amended in the Amendment dated December 3, 2008.

Amendments to Claim 1

Claim 1 is being amended to clarify the block queue feature. The amended claim now specifies a block queue that comprises a plurality of queuing physical address regions.

Also, it is specified that the block queue has a pointer to indicate a location of a second physical address region at the head of the block queue. If the physical address corresponding to the logical address as indicated by the WRITE instruction is in the non-erased state, the amended claim 1 now specifies the claimed device being arranged to locate the second physical address region in accordance with the pointer to thereby associate that second physical address region with the logical address region containing that logical address.

Additionally, amended claim 1 specifies that the claimed device is arranged to write the location of the first physical address region into the location to which the pointer points and to move the pointer in a round-robin manner to indicate a location of a next one of the plurality of queuing physical address regions so that the location of that first physical address region is placed at a rear of the block queue, after the address mapping table is modified.

Basis for the amendment to claim 1 is found at page 14, lines 13-24 of the published international application.

Response to the Obviousness Rejection

As amended, claim 1 now expressly defines a structure for the block queue as being made up of a plurality of queuing physical address regions and having a pointer to indicate a location of a physical address region at the head of the block queue. Furthermore, this pointer moves in a

round-robin manner to indicate a location of a next one of the plurality of queuing physical address regions, after the address mapping table is modified. In contrast to the device as currently defined in claim 1, US 5,404,485 (''Ban'') is completely silent on such a block queue.

In the Advisory Action, the Examiner has presented the following observation with respect to Ban:

> Ban discloses a list including a physical memory address corresponding to a logical memory region, and modifying such physical to logical correspondence on need basis. *The examiner interprets that a new physical memory address corresponding to the logical memory region after the modification is stored in a head of the list (''head of the queue'').* (Emphasis added)

The applicants cannot agree with the Examiner's observation about Ban. It appears that the "list" of Ban referred to by the Examiner — as shown at 35 in Figure 5 - relates to a "logical unit table" that merely translates the logical unit number to a physical unit number for a logical unit; see column 5 lines 13-14. Such a "list" of Ban is clearly not a block queue as now defined in claim 1, since the "list" of Ban does **not** have any pointer which indicates a location of an available address let alone such a pointer that moves in a round-robin manner to indicate a location of a next available address in the block queue.

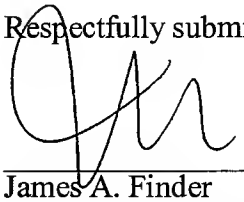
The "write" operations as performed by Ban's device are described at column 5, line 36, to column 6, line 2. Specifically, if a block of memory to which data is to be written is in a "non-erased" state, Ban teaches an algorithm for scanning the block allocation maps for each unit **until** a free block is located. The status of the original block of memory is then updated to "deleted" while the status of the located free block is updated to "written". Ban then goes on to explain, with reference to the flow diagram of Figure 6, the scanning of the unit allocation tables if a logical address is in the "non-erased" state. Once a free address is found from the unit allocation table, the status of the original block of memory is updated to "deleted" while the status of the located free block is updated to "written".

Clearly, however, Ban does **not** teach that a free block (or address) located by the scanning algorithm is in accordance with any pointer which indicates a location of an available block (or address) at a head of a block queue, let alone such a pointer that moves in a round-robin manner to indicate a location of a next available address in the block queue. On the contrary, it is clear that Ban's free block (or address) relates to the **first** block (or address) that has been found by the scanning algorithm to be "free" for mapping to a logical address, since the scanning algorithm executes **only until** the free block is located.

By providing a block queue having a pointer which indicates a location of a physical address region at a head of the block queue and which moves in a round-robin manner to indicate a location of a next one of a plurality of queuing physical address regions, embodiments of this device may ensure that the different blocks of the memory are used on a comparable frequency. This minimizes a quicker wearing out of certain blocks of the memory due to a higher usage frequency than other blocks. By contrast, certain blocks/addresses of the memory in the device of Ban are likely to be used more frequently than other blocks/addresses since Ban teaches that the physical memory space is "reclaimed periodically"; column 6, lines 4-5. Consequently, the free blocks/addresses that are more frequently found by the scanning algorithm will be used to store data more frequently, compared with the free blocks/addresses that are less frequently found. This leads to a quicker wearing out of the free blocks (or addresses) that are more frequently used to store data.

In view of the foregoing arguments, the invention of claim 1 is not obvious over Ban considered with the other cited art, at least in respect of the block queue feature as now claimed. Accordingly, the invention as defined in claims 1-15 and 17-21 is patentable over the cited prior art and allowance is requested.

Respectfully submitted,



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